CLAIMS

What is claimed is:

1. A serially programmable integrated circuit (IC) comprising:

a memory array comprising a plurality of primary columns and a plurality of redundant columns, the plurality of primary columns being organized into a plurality of primary column groupings, each having a first width, and the plurality of redundant columns being organized into a plurality of redundant column groupings, each having the first width;

a plurality of redundant register circuits, each comprising a redundant cascaded shift register having the first width;

a plurality of primary register circuits, each comprising a primary cascaded shift register having the first width;

a bitline latch comprising a plurality of primary bitline latch groupings and a plurality of redundant bitline latch groupings, each of the primary bitline latch groupings being coupled between a corresponding primary cascaded shift register and a corresponding one of the primary column groupings, and each of the redundant bitline latch groupings being coupled between a corresponding redundant cascaded shift registers and a corresponding one of the redundant column groupings; and

bypass logic for selectively daisy-chaining the redundant cascaded shift registers and the primary cascaded shift registers.

2. The serially programmable IC of Claim 1, wherein each of the plurality of primary register circuits further comprises a primary input terminal and a primary output terminal, and wherein the bypass logic comprises a primary multiplexer in each primary register circuit, the primary multiplexer in each primary register circuit comprising:

a primary multiplexer output terminal coupled to the primary output terminal;

a first primary multiplexer input terminal coupled to the primary input terminal;

a second primary multiplexer input terminal, the primary cascaded shift register being coupled between the primary input terminal and the second primary multiplexer input terminal; and

a primary multiplexer control terminal for selectively connecting one of the first primary multiplexer input terminal and the second primary multiplexer input terminal to the primary multiplexer output terminal.

3. The serially programmable IC of Claim 2, wherein each of the plurality of redundant register circuits further comprises a redundant input terminal and a redundant output terminal, and wherein the bypass logic comprises a redundant multiplexer in each redundant register circuit, the redundant multiplexer in each redundant register circuit comprising:

a redundant multiplexer output terminal coupled to the redundant output terminal;

a first redundant multiplexer input terminal coupled to the redundant input terminal;

a second redundant multiplexer input terminal, the redundant cascaded shift register being coupled between the redundant input terminal and the second redundant multiplexer input terminal; and

a redundant multiplexer control terminal for selectively connecting one of the first redundant multiplexer input terminal and the second redundant multiplexer input terminal to the redundant multiplexer output terminal.

4. The serially programmable IC of Claim 3, wherein the plurality of primary register circuits are daisy-chained together, and wherein the redundant register circuits are daisy-chained together, the primary output terminal of one of the plurality of primary register circuits being coupled to the redundant input terminal of one of the plurality of redundant register circuits.

5. The serially programmable IC of Claim 4, wherein the one of the plurality of primary register circuits is a last one of the plurality of primary register circuits, and wherein the one of the plurality of redundant register circuits is a first one of the plurality of redundant register circuits.

6. The serially programmable IC of Claim 3, wherein the plurality of primary register circuits are daisy-chained together, and wherein the redundant register circuits are daisy-chained together, the primary input terminal of one of the plurality of primary register circuits being coupled to the redundant output terminal of one of the plurality of redundant register circuits.

7. The serially programmable IC of Claim 4, wherein each of the primary register circuits further comprises a primary multiplexer control circuit coupled to the primary multiplexer control terminal, and wherein each of the redundant register circuits further comprises a redundant multiplexer control circuit coupled to the redundant multiplexer control terminal.

8. The serially programmable IC of Claim 7, wherein the primary multiplexer control circuits and the redundant multiplexer control circuits comprise non-volatile programmable circuits.

9. The serially programmable IC of Claim 7, further comprising an output control circuit for reading a data word out of the memory array, the output control circuit comprising:

a defective address circuit for identifying primary column groupings that include defective columns and redundant column groupings that contain stored data;

a redundant output control circuit for shifting data out of redundant column groupings identified by the defective address circuit as containing stored data; and

a primary output control circuit for shifting data out of primary column groupings not identified by the defective address circuit as including defective columns.

10. The serially programmable IC of Claim 9, wherein the primary output control circuit comprises:

a plurality of primary sense amplifiers;

a column select circuit for coupling the plurality of primary sense amplifiers to selected primary columns in the memory array;

a plurality of primary data latches for latching data sensed by the plurality of primary sense amplifiers; and

a primary bit shifting multiplexer for serially shifting out data latched in the plurality of primary data latches.

11. The serially programmable IC of Claim 10, wherein the plurality of primary data latches have a total width equal to a second width, and wherein the column select circuit comprises a column address generator for generating a sequence of column addresses, each of the column addresses corresponding to a portion of the primary columns, the portion of the primary columns having the second width.

12. The serially programmable IC of Claim 11, wherein the plurality of primary data latches are organized into primary latch groupings, each of the primary latch groupings having the first width, and wherein the primary bit shifting multiplexer comprises:

a plurality of primary pass transistor pairs, each of the primary pass transistor pairs including a first pass transistor and a second pass transistor serially coupled between one of the plurality of primary data latches and an output terminal of the serially programmable IC, the plurality of primary pass

transistor pairs being organized into a plurality of primary pass transistor groupings, each of the primary pass transistor groupings being associated with one of the primary latch groupings;

a shifting signal generator for generating a repeating cycle of shifting signals, each of the shifting signals turning on one of the second pass transistors in each of the primary pass transistor groupings;

a word address generator for generating a sequence of word addresses, each of the word addresses corresponding to one of the plurality of primary latch groupings, the word address generator incrementing the word address after each cycle of the shifting signals; and

a first binary decoder for decoding the word address into a word select signal, the word select signal turning on the first pass transistor for all pass transistor groupings associated with one of the plurality of primary latch groupings.

13. The serially programmable IC of Claim 12, wherein the defective address circuit includes a plurality of defective address memories for storing the location of primary column groupings that include defective columns, each location being based on a predetermined column address and a predetermined word address, and wherein the word address generator comprises a checking circuit for performing a bypass operation on an upcoming one of the sequence of column addresses and an upcoming one of the sequence of word addresses, the bypass operation comprising instructing the word address generator to bypass the

upcoming one of the sequence of word addresses when the upcoming one of the word addresses matches the predetermined row address and the upcoming one of the sequence of column addresses matches the predetermined column address.

14. The serially programmable IC of Claim 13, wherein the checking circuit performs the bypass operation during each cycle of the shifting signals, and wherein the checking circuit completes each bypass operation within a single cycle of the shifting signals.

15. The serially programmable IC of Claim 13, wherein the redundant output control circuit comprises:

a plurality of redundant sense amplifiers;

a plurality of redundant data latches for latching data sensed by the plurality of redundant sense amplifiers;

a redundant bit shifting multiplexer for serially shifting out data from the plurality of redundant data latches.

16. The serially programmable IC of Claim 15, wherein the plurality of redundant data latches are organized into redundant latch groupings, each of the redundant latch groupings having the first width,

wherein the redundant bit shifting multiplexer comprises a plurality of redundant pass transistor pairs, each of the redundant pass transistor pairs including a first redundant pass transistor and a second redundant pass transistor serially coupled between one of the plurality of redundant latches and the output terminal of the serially programmable IC, the plurality of redundant pass transistor

pairs being organized into a plurality of redundant pass transistor groupings, each of the redundant pass transistor groupings being associated with one of the redundant latch groupings, wherein each of the shifting signals from the shifting signal generator turns on one of the second redundant pass transistors in each of the redundant pass transistor groupings, and

wherein each of the defective address memories includes a redundancy enable bit for identifying redundant pass transistor groupings associated with redundant column groupings having stored data, the redundant bit shifting multiplexer comprising a redundancy read circuit for generating a sequence of redundant column enable signals, each of the sequence of redundant column enable signals turning on all the first redundant pass transistors for one of the redundant pass transistor groupings.

17. A serially programmable integrated circuit (IC) comprising:

a memory array including primary columns organized into primary column groupings having a first width and redundant columns organized into redundant column groupings having the first width;

a plurality of primary data registers having the first width, the plurality of primary data registers being daisy-chained by primary register bypass logic, the primary register bypass logic selectively including or bypassing the primary data registers in a serial programming path for the IC;

a plurality of redundant data registers having the first width, the plurality of redundant data registers being daisy-chained by redundant register bypass logic,

the redundant register bypass logic selectively including or bypassing the redundant data registers in the serial programming path; and

a bitline latch, the bitline latch comprising a plurality of primary latch groupings and a plurality of redundant latch groupings, each of the primary latch groupings having the first width, each of the primary latch groupings being associated with one of the plurality of primary data registers and one of the plurality of primary column groupings, and each of the redundant latch groupings having the first width, each of the redundant latch groupings being associated with one of the plurality of redundant data registers and one of the plurality of redundant column groupings.

18. The serially programmable IC of Claim 17, wherein the primary register bypass logic and the redundant register bypass logic comprise non-volatile programmable logic for bypassing or including the primary data registers and the redundant data registers, respectively, in the serial programming path.

19. The serially programmable IC of Claim 18, further comprising means for reading a data word out of the memory array, the means for reading the data word comprising:

means for identifying primary column groupings that include defective columns and redundant column groupings that contain stored data;

means for shifting a first portion of the data word out of the redundant column groupings that contain stored data; and

means for shifting a second portion of the data word out of the primary column groupings that do not include defective columns.

20. The serially programmable IC of Claim 19, wherein the IC comprises an output terminal, and wherein the means for identifying comprises means for storing a plurality of redundancy column indicators, each of the redundancy column indicators identifying a redundant column grouping that contains stored data, and wherein the means for shifting the first portion of the data word out of the redundant column groupings comprises:

means for latching data from the redundant column groupings into a plurality of redundant data latches, the redundant data latches organized into a plurality of redundant output latch groupings, each of the redundant output latch groupings being associated with one of the redundant column groupings;

means for generating a bit shifting signal; and

means for sequentially shifting data out from the redundant output latch groupings associated with redundant column groupings identified by the redundancy column indicators to the output terminal in response to the bit shifting signal.

21. The serially programmable IC of Claim 20, wherein the means for identifying further comprises means for storing a plurality of defect addresses, each of the defect addresses identifying a primary column grouping that includes defective columns, and wherein the means for shifting the second portion of the data word out of the primary column groupings comprises:

means for assigning a local address to each of the plurality of primary column groupings;

means for latching data from the primary column groupings into a primary bitline latch;

means for sequentially shifting data out from the primary output latch groupings to the output terminal in response to the bit shifting signal, the means for sequentially shifting data out from the primary output latch groupings comprising means for bypassing data from primary column groupings having local addresses that match any of the defect addresses.

22. The serially programmable IC of Claim 21, wherein the means for bypassing data comprises lookahead means for detecting and bypassing primary column groupings having local addresses that match any of the defect addresses before the means for sequentially shifting data out from the primary output latch groupings attempts to shift data out from the primary column groupings having local addresses that match any of the defect addresses.

23. A method for configuring an integrated circuit (IC) comprising:

testing a plurality of primary column groupings in a memory array in the IC to detect defective columns;

programming a bypass logic circuit to bypass one or more primary data registers in a serial programming path, wherein each of the one or more primary data registers bypassed by the bypass logic circuit is associated with a primary column grouping including a defective column;

programming the bypass logic circuit to incorporate one or more redundant data registers in the serial programming path for each of the one or more primary data registers bypassed by the bypass logic circuit, wherein each of the one or more redundant data registers is associated with a redundant column grouping in the memory array;

serially shifting data into the primary data registers and redundant data registers in the serial programming path; and

loading data from the primary data registers and the redundant data registers in the serial programming path into the memory array in parallel.

24. The method of Claim 23, further comprising:

programming a defective address into an output control circuit of the IC for each of the primary data registers bypassed by the bypass logic circuit; and

programming a redundancy enable indicator into the output control circuit for each of the redundant data registers incorporated into the serial programming path by the bypass logic circuit.

25. A method for programming a serially programmable integrated circuit (IC), the IC comprising an input terminal, a plurality of primary data registers, a plurality of redundant data registers, a bitline latch, and a memory array including a plurality of primary column groupings and a plurality of redundant column groupings, each of the plurality of primary column groupings being coupled to receive programming data from one of the plurality of primary data registers bit the bitline latch, and each of

the plurality of redundant column groupings being coupled to receive programming data from one of the plurality of redundant data registers via the bitline latch, the method comprising:

shifting a programming bitstream into the primary data registers through the input terminal;

bypassing primary data registers associated with primary column groupings that include defective columns;

shifting the programming bitstream into the redundant data registers until the programming bitstream is completely shifted through the input terminal;

latching data from the primary data registers and redundant data registers into the bitline latch; and

programming data from the bitline latch into the memory array.